1. (Twice Amended) An integrated circuit package comprising:

an integrated circuit die, said integrated circuit die having a top side and a bottom side opposite said top side, said top side including at least one bond pad;

at least one raised interconnect located over and conductively coupled to said at least one bond pad; and

a solid flexible dielectric circuit film having a top surface, a bottom surface and a routing conductor, the flexible circuit film having at least one outer landing formed on the top surface and at least one inner landing formed on the bottom surface such that the landings on the top and bottom surfaces are fully supported by the circuit film, wherein the outer landing is laterally offset from the inner landing and the two landings are connected via the routing conductor, which extends laterally within the solid flexible dielectric circuit film,

wherein the flexible circuit film being located over and conductively attached to at least one raised interconnect such that an air gap is formed between said integrated circuit die and said flexible circuit film.

15. (Twice Amended) An integrated circuit wafer having a top side and a bottom side opposite said top side, said integrated circuit wafer comprising:

a plurality of integrated circuit dice, said plurality of integrated circuit dice having a plurality of bond pads located on said top side of said integrated circuit wafer;

a plurality of raised interconnects formed over and conductively coupled to said plurality of bond pads; and

a solid flexible dielectric circuit film having a top surface, a bottom surface and routing conductors, the flexible circuit film having a plurality of outer landings located on the top surface and a plurality of inner landings located on the bottom surface such that the landings on the top and bottom surfaces are fully supported by the circuit film, wherein the individual outer landings are laterally offset from the individual inner landings and the landings are connected via routing conductors, which extend laterally within the solid flexible dielectric circuit film,

wherein the flexible circuit film being located over and conductively attached to the plurality of raised interconnects such that an air gap is formed between said integrated circuit wafer and said flexible circuit film.